Date: Thu, 8 Jul 93 09:38:40 PDT
From: Packet-Radio Mailing List and Newsgroup <packet-radio@ucsd.edu>
Errors-To: Packet-Radio-Errors@UCSD.Edu
Reply-To: Packet-Radio@UCSD.Edu
Precedence: Bulk
Subject: Packet-Radio Digest V93 #201
To: packet-radio

Packet-Radio Digest   Thu, 8 Jul 93   Volume 93 : Issue 201

Today's Topics:

Send Replies or notes for publication to: <Packet-Radio@UCSD.Edu>
Send subscription requests to: <Packet-Radio-REQUEST@UCSD.Edu>
Problems you can't solve otherwise to brian@ucsd.edu.

Archives of past issues of the Packet-Radio Digest are available
(by FTP only) from UCSD.Edu in directory "mailarchives/packet-radio".

We trust that readers are intelligent enough to realize that all text
herein consists of personal comments and does not represent the official
policies or positions of any party. Your mileage may vary. So there.

Date: Thu, 8 Jul 93 03:04:56 GMT
From: koriel!sh.wide!wnoc-snd-ss2!sakunami!gatortia!wapiko!jf7pbw!jf7wex!
jf7wex@ames.arpa
Subject: advanced packet radio in Japan
To: packet-radio@ucsd.edu

In article <C9qyKI.KoL@srgenprp.sr.hp.com>
     glenne@sr.hp.com (Glenn Elmore) writes:

 Glenn,

|I'm not sure of IQ modulation in conjunction with the two parts you
|mention but I've had very good luck at building an IQ modulator for
|1200 MHz directly on PC board.

In RF 2802 or 2402, IQ input pins are connected to DBM simply via
differential amplifier for each.

I will appriciate it if you would describe your modulator.
And if the modulator is using rat-race-type mixer, 3dB hybrid mixer,
or something similar with phase splitter, especially about phase splitter.
(The both mixers are made of an microstrip square or circle on board
with two diodes.)

Easy to obtain 2Mbps QPSK demod chip, nobody I know has built high speed
QPSK modulator in Japan. To achieve it, I am studying digital radio
communication espc. modulators and demodulators in both theory and
actual imprement and SS as well.
Will you tell me some books suitable for it?
(Books published with the company that have the office in Japan,
such as McGraw-Hill or Prentice Hall, must be easy to buy.)

Thanks,
73

Ryuji Suzuki, JF7WEX
Packet Radio User's Group, PRUG

Date: Thu, 8 Jul 93 02:48:42 GMT
From: koriel!sh.wide!wnoc-snd-ss2!sakunami!gatortia!wapiko!jf7pbw!jf7wex!
jf7wex@ames.arpa
Subject: advanced packet radio in Japan
To: packet-radio@ucsd.edu

In article <1993Jul6.175415.27229@nrao.edu>
     dvarney@jabbah.NoSubdomain.NoDomain (DOUGLAS VARNEY) writes:

| I read with great interest your description of PRUG activities
| posted to r.r.a.packet. I was especially interested with the
| mention of a ic for QPSK at 2Mbps by Toshiba. Could you tell
| me what the part nubere is ? I have need of something like this
| at 2.11Mbps and 644Kbps.

Thank you for your interest in PRUG's.
The number is TB1202N/F. Suffix N means DIP and F means
surface mounting (flat) package. This works at a 5V supply.
And there is TA7782N, probably works similar to TB1202, requires two
voltages of supplying.

According to data sheet of TB1202, it takes externally two crystals,
for VCXO locking carrier and symbol rate, and some RCs as loop filters.
No more parts seems needed to output serialized data, and 192fs
or 384fs clock.

These chips are for satelite broadcasting reciever in SHF and
I am not sure of whether the same format is used world-wide.
NICAM (Near Instantaneous Compouned Audio Multiplex), also same QPSK
but slower speed, is used on earth in the UK and the Scandinavian.

|P.S. I tried you internet address, but no luck (bounced)

Sorry, that address cannot recieve from out of Japan, yet.
jf7wex@zao.gw.tohoku.ac.jp can. This article includes
reply-to line with this address.

73

Ryuji Suzuki, JF7WEX
Packet Radio User's Group, PRUG

Date: Thu, 8 Jul 1993 16:05:24 GMT
From: dog.ee.lbl.gov!overload.lbl.gov!agate!howland.reston.ans.net!math.ohio-state.edu!sdd.hp.com!col.hp.com!news.dtc.hp.com!srgenprp!glenne@network.UCSD.EDU
Subject: advanced packet radio in Japan
To: packet-radio@ucsd.edu

Ryuji Suzuki (jf7wex@jf7wex.sdj.miyagi.prug.or.jp) wrote:

: In RF 2802 or 2402, IQ input pins are connected to DBM simply via
: differential amplifier for each.

  I've had good luck using differential ECL logic (10116 variety) to drive DBMs directly. They have adequate current capability along with good balance and speed. I've used this to direct sequence modulate a variety of Schottkey diode mixers. I am interested if you have a good and simple discrete transistor design though.

: I will appriciate it if you would describe your modulator.
: And if the modulator is using rat-race-type mixer, 3dB hybrid mixer,
: or something similar with phase splitter, especially about phase splitter.
: (The both mixers are made of an microstrip square or circle on board
: with two diodes.)

  Yes, I use 6/4 lambda, rat race mixers which I've folded to reduce board space. The first mixer is driven by the PN generator for spreading and de-spreading. The other two mixers are driven by a Wilkinson power divider from the previous mixer on the signal port and by a 90 degree hybrid on the LO side. This phase splitter is also folded to reduce board area. For good amplitude accuracy the line widths/impedances need to be pretty well controlled. So far, I've built

everything at home in the ham shack but still get phase accuracy within a degree or two. Amplitude accuracy hasn't been quite as good but is also not quite as sensitive since this is on the LO side and I am saturating the mixer diodes. The entire assembly is about 10 X 12 cm on standard epoxy/fiberglass board.

I'm using dual, packaged surface mount diodes and SMT resistors/capacitors for the termination of the hybrid and DC blocking. Parts cost is extremely low. I'm floating each mixer so that I can drive them differentially from a single supply. RF grounds for the termination and IFs are provided by radial transmission lines (fan lines).

So far, my main use for the I/Q modulation capability has been to generate a SSB pilot tone(above the data). The system I'm building phase locks on a pilot tone in order to be able to do coherent detection. To date, I've only modulated data on both mixers together rather than making use of the full I/Q capability. Because I'm choosing channel coding with no DC component, the spectrum near the carrier is free for other uses. It seems that a simple 90 degree audio hybrid would give a coherent SSB audio channel as well, almost for free. I haven't decided what to use it for yet though (:>)

My spreading sequence operates synchronously with the carrier/pilot and data clocks. Therefor, once I have acquired PN synchronization (by software rather than a hardware loop) and have locked onto the pilot tone, everything stays locked and synchronous and I also have all data clocks recovered.

I'm generating the carrier, at 1265 MHz, in one half of a dual PLL chip. The second half is used to phase lock the master VCXO (at 31.47 MHz) to the received pilot tone. The carrier oscillator uses a coaxial line resonator and results in very low phase noise. See my 1988 Ham Radio Magazine microwave series for a similar design.

Thus the system is direct conversion and fully synchronous and the RF portion is largely printed on PC board so it is also almost "no-tune". The spreading can be turned on or off as desired. I haven't finished the low level stages of the RF chain but I'm trying to use standard MMICs and a simple diode attenuator arrangement which I can turn around for power/gain control between transmit and receive. The filtering is done by an interdigital filter (not printed but using the same sort of resonators as the 1265 VCO) which is in the middle of these low level stages. I'm only trying for .5-1 watt on the main board but have already built a 20W PA with T/R switch which can be added. My goal is to be able to build the low power portion cheaply enough that additional radios/hops can be added rather than the P/A.

The goal of the radio is 250 Kbps data to the user. See our paper in the 9th ARRL CNC for a description of the Hubmaster protocol which supports this. The addition of spread spectrum and fully synchronous and coherent radios will require some additions to this protocol but the fundamental operation is similar.

: Easy to obtain 2Mbps QPSK demod chip, nobody I know has built high speed
: QPSK modulator in Japan. To achieve it, I am studying digital radio
: communication espc. modulators and demodulators in both theory and
: actual imprement and SS as well.
: Will you tell me some books suitable for it?
: (Books published with the company that have the office in Japan,
: such as McGraw-Hill or Prentice Hall, must be easy to buy.)

I haven't focussed much on channel coding yet. I've tried BPSK but I agree that QPSK could be a good addition and inexpensive chips to perform this would be great. If you have literature, or can point me toward some, I'd like to take a look at these parts. Hopefully they are available outside of Japan.

I'm not sure that I can help suggest the best books. I'm still in need of learning a lot myself. You might look for some of the texts authored/edited by Kamilo Feher and published by Prentice Hall. Those should be available.

I expect that most of the narrower bandwidth channel coding schemes (for NADC,JDC,CDMA etc) are beginning to be done digitally and then applied to the I/Q modulator.

I believe that the GMSK modulator in the GRAPES 56 kbps modem works this way. Of course, this starts to be more of a problem for amateurs at higher data rates.

73
Glenn Elmore n6gn

N6GN @ K3MC
amateur IP: glenn@SantaRosa.ampr.org
Internet: glenne@sr.hp.com

Date: 7 Jul 93 15:08:10 GMT
From: usc!howland.reston.ans.net!darwin.sura.net!rsg1.er.usgs.gov!news.cs.indiana.edu!bsu-cs!news.nd.edu!nova!jonathan@network.UCSD.EDU
Subject: Minisport Hacker - for those interested
To: packet-radio@ucsd.edu

Anthony J Stieber (anthony@csd4.csd.uwm.edu) wrote:

> All volumes of the MiniSport Laptop Hacker are available via anonymous
>ftp on the Internet as csd4.csd.uwm.edu:/pub/Portables/minisport.laptop.hacker.
> This directory contains many other files of interest to the portable
> computer user. See the INDEX file for a descriptions of most of the
> files.

> For those who aren't on the Internet I can mail any requested files.

> This service is provided free of charge.

Volumes 1 thru 8 are on the FTP site under 'minisport.laptop.hacker' but
where are volumes 9 thru 15? They are NOT there.

--
Jonathan Bradshaw | Email Jonathan.Bradshaw@nd.edu | Prodigy XMSN02B | Ham N9OXE
  WNDU-AM/FM/TV South Bend, IN | Disclaimer "My opinions are not my employers"
"If any girl rejects you, don't you doubt it's part of the .plan"-Deborah Gibson

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Date: 8 Jul 93 14:36:41 GMT
From: olivea!isc-br!tau-ceti!comtch!opus-ovh!bmork@uunet.uu.net
Subject: MiniSport Hacker - Vol 13 reissue
To: packet-radio@ucsd.edu

MiniSport Laptop Hacker - Vol 13, 29 Apr 1993

>>> ADMIN
No, I'm not superstitious, but the number of this MLH edition did pass my
mind. The last two weeks, my ZL-2 has been out of commission. Almost si-
multaneously, I received a letter from n7ftm (Bill) that his is having the
same trouble. I've spent the last few nights tearing mine apart. Bad for
me; good for you! I've got more specs on how the power supply works in
the next edition of MLH.

In addition, I've been digesting volumes of documentation on Internet and
Waffle, a BBS program meant to host users and process Internet E-mail and
Usenet topical forums. I now have a node running on my own computer. See
the new (and let's hope stable) address below.

Two people have sent me messages via USMail because something about the
packet link wasn't getting messages through. Each edition, I try to con-
firm in the ADMIN section who all I've heard from. If I don't mention
your callsign here, I didn't get your message. This round I've heard from
N9ADS, N9LNQ, WA8WZX, W4NTG, W5SYT, N7FTM, KA9CAP.

>>> COM I/O ARCHITECTURE

Continuing from Volumes 7,8, and 10, there are only three more registers to cover.

Line Control Register (LCR) at address (BASE+3)

This register allows you to configure the format of the serial data leaving the UART and (simultaneously) the format expected by the UART. All bits of this register are read/write.

Bit 0&1: These two bits select how many data bits are transferred in each asynchronous character. 5,6,7, or 8 bits are selected with values of 00,01,10, or 11 respectively. For example, if you desire 7 data bits, set Bit0 to 0 and Bit1 to 1.

Bit 2: Set to 0 if you want one stop bit generated on outbound data and checked on inbound data. Setting to 1 chooses 1-1/2 stop bits with 5-bit data and two stop bits with 6,7, or 8-bit data.

Bit 3: Set to 1 to generate a parity bit. Set to 0 if you want no parity bit at all. If this is set to 0, the next bit has no effect.

Bit 4: Even Parity Select. When Bit3 is 1 and Bit4 is 0, an odd number of 1's is transmitted or checked in the data bits and parity bit. When Bit3 is a 1 and Bit4 is a 1, an even number of bits is transmitted or checked.

Bit 5: When set to 1, the function of Bit4 is reversed.

Bit 6: Set Break. When this bit is set to 1, the serial output is forced to the spacing state (same as data=0) and remains until changing this bit to a 0.

Bit 7: This is the Baud-Rate Divisor Latch Access Bit. This bit is set to 0 for normal operation allowing access of the transmitter and receiver buffers at BASE+0, and the Interrupt Enable Register at BASE+1. When set to 1, these same addresses access the Baud Rate Divisor.

Line Status Register (LSR) at address (BASE+5)

This register provides information about recent data transfer. All bits are not read/write.

Bit 0: Data Ready. The UART sets this bit to 1 whenever a complete incoming character is available in the receiver buffer. It is reset to 0 by writing a zero or by reading the receiver buffer. Bit1 through Bit4 are "errors" that produce a RLS interrupt (see IER and IIR descriptions).

Bit 1: Overrun. This bit is set to 1 whenever the receiver buffer was not read by the CPU before the next character was transferred into the receiver buffer (overwriting the lost character). This bit is reset to 0 whenever the CPU reads the LSR.

Bit 2: Parity Error. If this bit is 1, the received character did not have the correct even or odd parity as selected by the bits in the LCR. It resets to 0 whenever the CPU reads the LSR.

Bit 3: Framing Error. This bit is set to 1 whenever the stop bit following the last data bit (or parity, if selected) is detected in the spacing level. (A stop bit is suppose to be mark status.)

Bit 4: Break Received. This is set to 1 whenever the received data input is held in spacing status longer than a full word's time: the total of start bit, data bits, parity, and stop bits.

Bit 5: Transmitter register empty. This bit is 1 when the UART is ready to accept a new character for transmission. It actually switches to 1 when the previous character is moved from the transmitter holding register to the transmit shift register. It becomes 0 concurrently with the loading of the holding register by the CPU.

Bit 6: Transmitter shift register empty. This bit is 1 whenever the shift register is idle (nothing being transmitted). It becomes 0 when the shift register gets a character from the transmitter holding register.

Bit 7: Permanently 0

Baud Rate Divisor Latch at addresses (BASE, BASE+1)

These two registers set the bits per second rate transmitted by the UART. This is a 16-bit divisor for the clock fed into pin 16 of the 8250 UART, giving a frequency *sixteen* times the desired baud rate. Pin 16 is usually fed with a frequency of 1.8432 MHz.

The LSB (least significant byte) is written to (or read from) address BASE, and the MSB (most significant byte) is written/read from address BASE+1. This is true only when the Divisor Access Bit in the LCR is set to 1.

The following table can be used if a 1.8432 Mhz clock is used (table values are decimal):

	300	1200	2400	4800	9600	19200
MSB	1	0	0	0	0	0

LSB 128   96   48   24   12   6

Lastly, a request: Please look in any data book you have and try to identify the following three chips. Two of each are surface mounted on the bottom side of the ZL power supply switching regulator board. I need to find out how they're suppose to work to know if mine are working! A pinout and short description would be GREATLY appreciated!

73, Brian Mork (Opus-OVH)   KA9SNF@wb7nnf.#spokn.wa.usa
                                  Internet ka9snf@opus-ovh.spk.wa.us
                                  6006-B Eaker, Fairchild, WA 99011

Brian Mork   Internet bmork@opus-ovh.spk.wa.us
 . . . .   Amateur Radio ka9snf@wb7nnf.#spokn.wa.usa
.. . ..   USMail 6006-B Eaker, Fairchild, WA 99011

Date: 8 Jul 93 14:37:57 GMT
From: olivea!isc-br!tau-ceti!comtch!opus-ovh!bmork@uunet.uu.net
Subject: MiniSport Hacker - Vol 14 reissue
To: packet-radio@ucsd.edu

MiniSport Laptop Hacker - Vol 14   25 May 1993

>>> ADMIN
Things have been pretty quiet this time around. I got only one message back from the field. In the meantime, I managed to bring up an Internet node in-house, and I'll start porting these newsletters over there, too. Look in the micro.zenith and rec.radio.amateur.packet forums. If you read these MiniSport Laptop Hacker newsletters, please make it a practice of kicking back at least a one line message indicating what parts are particularly useful or not useful.

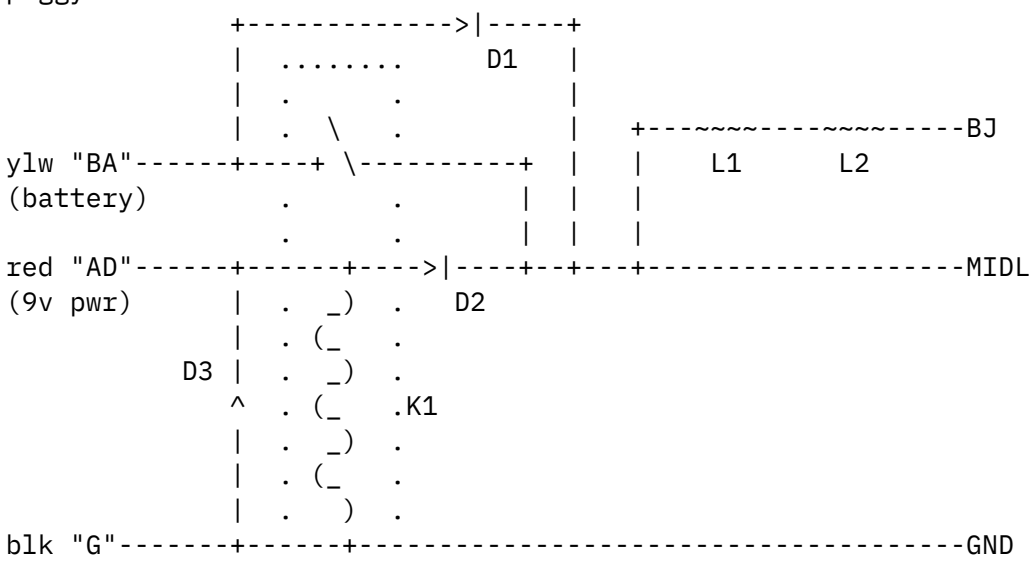
>>> POWER SUPPLY HARDWARE
Well, for those of you that have been following the MLH series, you'll know that one of my power supplies has been giving trouble. It finally gave up the ghost. Simultaneously I heard from another ham who had nearly identical symptoms: The Power & NumLock LEDs flash on for about 1/2 second and then the computer power downs by itself. From Internet, I heard from one person who bought his for a real price, with a guarantee. Its power supply died this way, also, and the seller replaced it. He's had no problems since. Too many similar stories! I wanted to know what's going on! In the meantime, I'm looking to buy broken MiniSports.

I tore mine open and started from the exterior working in. There are a handful of components that condition power and select where power is coming from --the AC adapter or the battery. This initial power supply section is documented below.

My two ZL-x computers are different:

Older	Newer
* Power supply piggyback card with number PA2020P25	* Power supply all on one card with number PA2020P65
* Motherboard 1PC1606AMB-40I with green patch wire from TP43	* Motherboard 1PC1606AMB-41I, no patchwire from/to Test Point 43.
* U47 BIOS is "BIOS V3.3D"	* U47 BIOS is "444-804"
* Disk controller WD37C65BJM has manufacture date in 22nd week of 1989.	* Disk controller is same part number dated 44nd week in 1989.

The power conditioning sections are physically different, but electrically they're the same. I expect my older one was a "fix-it" prototype that later made it onto the production board. Here's the schematic of the piggyback section:



D1,D2 - two B8300s or integral N9K-60QC04

D3 - ceramic bubble (part no. unknown)

L1 - approx 24 turns on 1/4" form

L2 - 1 turn on core

K1 - SPDT DIP relay, bottom view M * AD n/c * *

BJ named because the older power supply has a Blue Jumper wire.

MIDL named because it is the MIDDLE wire

```
                        pinout:   |              connecting the piggy-
                                  *    *  *      back board.
                                      GND BA
```

Operating from battery power, power comes in through D1 and out both the BJ and MIDL connections. When the 9v is available, current comes in through D2, again going out BJ and MIDL. My suspicion is that one of these carries the main power current and one is a monitor tap, i.e., indicates when AC sourced power (9v) is available. Additionally, K1 pulls the contact closed, providing current back to the battery pack for charging. If you listen carefully when 9v is connected, you can hear K1 click closed. the glass diode (D2) provides a shorted path for the current spike coming from K1 when it clicks off.

Notice that this circuit is in operation whether or not the computer is turned "on." It might be more appropriate to think of the computer as always being on; when you press the on button, the power supply just "upgrades" to full output status. The rest of the power supply (all stuff between what I presented above and the header I described back in issue ????) lives on an approximately 5"x4" circuit board. Reverse engineering of this board has been slowed by my inability to identify three chips. There are two of each of the following: MB3778 (16-pin IC), K612 (3-terminal + heat sink tab), and D4049G (16-pin IC). PLEASE FORWARD ANY INFORMATION YOU HAVE ON THESE THREE CHIPS.

73, Brian, ka9snf@wb7nnf.#spokn.wa or Internet bmork@opus-ovh.spk.wa.us

---

Brian Mork Internet bmork@opus-ovh.spk.wa.us
 . . . . Amateur Radio ka9snf@wb7nnf.#spokn.wa.usa
.. . .. USMail 6006-B Eaker, Fairchild, WA 99011

Date: 8 Jul 93 14:38:52 GMT
From: olivea!isc-br!tau-ceti!comtch!opus-ovh!bmork@decwrl.dec.com
Subject: MiniSport Hacker - Vol 15
To: packet-radio@ucsd.edu

MiniSport Laptop Hacker - Vol 15 7 July 1993

>>> ADMIN

This month has been busy! I've been installing (definitely progressive tense English --these things seem to never end :) an Internet node and that has taken a lot of time. Watch the comp.sys.zenith and rec.radio.amateur.packet newsgroups for future issues of MLH if you're on Internet. Exposure on that net created a flood of feedback. The biggest feedback item? MiniSports fail by loosing their power supply. I'm still

working on the project from last issue --restoring my busted power supply.

This issue is sent out with R95 on those nets that require it. R95 is a neat program that automatically splits and reassembles large files. Let me know if it works for you before I terminate the "trial run" and commit to using it long term. If you'd like a copy and you're Internet capable, I'll send you a UUENCODEd copy. If you're Amateur Packet only, I can copy stuff onto disk if you make it a no-cost option for me. I'll put a variety of other MLHacker related goodies on there, too.

Flying for the Air Force is my primary job. They're sending me TDY to Saudi Arabia again, which will knock out all this fun stuff until mid-September. Look for Volume 16 at about that time.

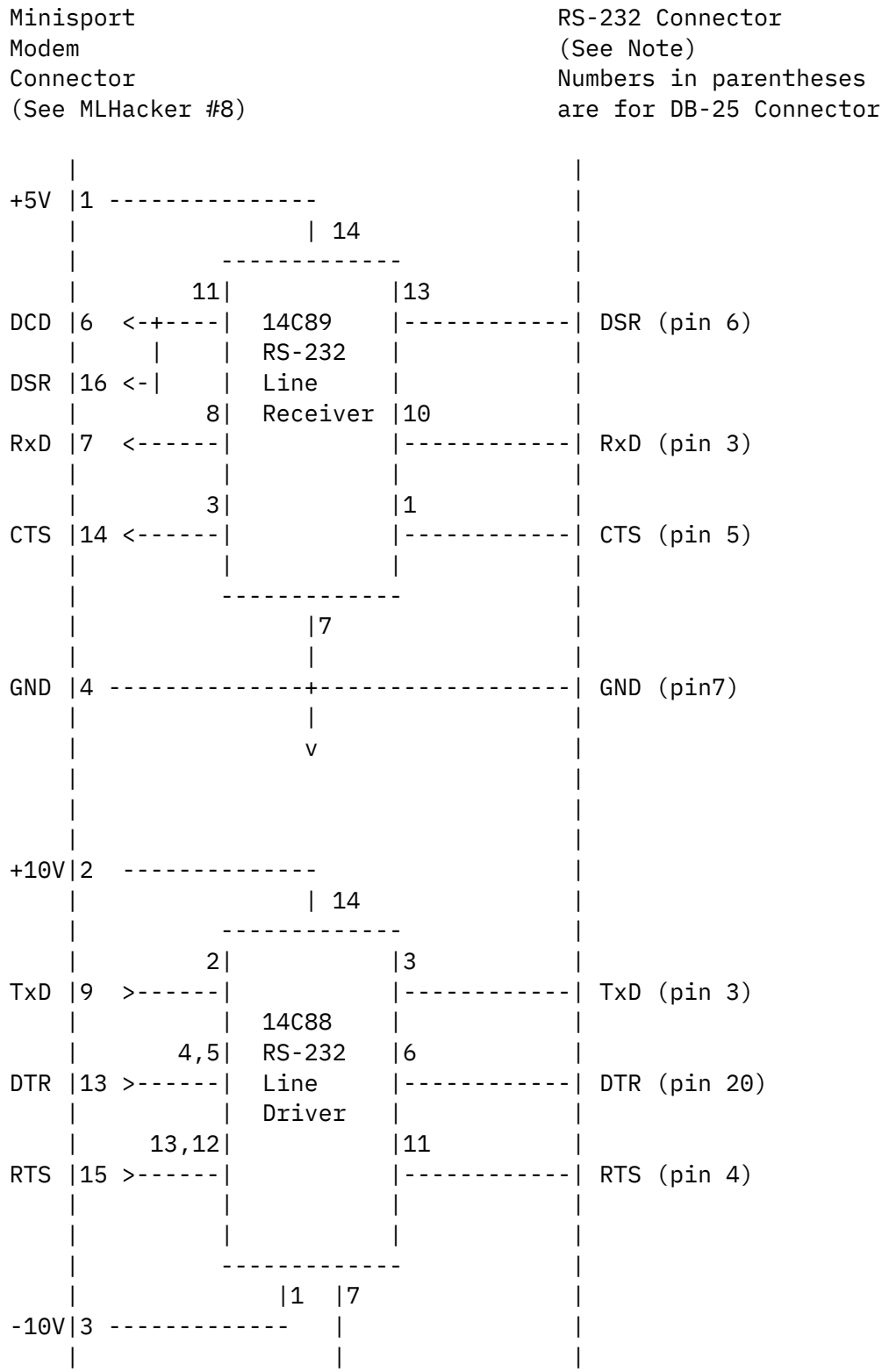
>>> RESOURCES
I came across three articles you may be interested in. The first is "Real World Portability," in Oct 1989 REMark, written by Nathan Baker. It is a product review of the Minisport when it just came out on the market (you don't want to know the initial price!). In the same issue, William M. Adney writes "On the Leading Edge" which featured the Minisport as one step in ZDS's progression on the frontier of new system designs. The third article, "The Care and Feeding of MinisPorts," by Mary Ellen Shutz, appears in the July 1991 issue of REMark. It discusses power management, an expanded and more authoritative version of MLH Volume 11. After reading the third article, I notice an error on my part. Using SLOW mode in the SETUP is not the same as invoking SLOW mode via the FN-F3 keyboard sequence. The SETUP option actually chooses between 8 MHz and 4.77 MHz operation, but the keyboard sequence just inserts wait states to slow the system down. REMark is the official Zenith Data Systems magazine.

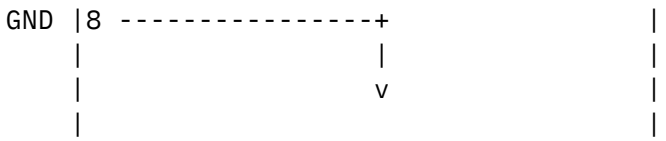
>>> TECH HELP REQUESTED
I have the PMP (Poor Man's Packet) running in the modem slot of my Minisport, thanks to the help of a local ham (Ron, N7SXD). The receive works fine, but upon transmit, the software chokes. I'm convinced that on the Minisport, the algorithms coded in C just aren't fast enough. Has anybody out there rewritten critical sections in assembly?

>>> DOUBLE YOUR SERIAL PORT COUNT
This schematic came in via Internet. Thank you Peter (N9IYJ)! It connects into the internal modem header and converts it from a TTL port to a standard PC compatible serial port. Quoting Peter...

"Following is an attempt at an ASCII schematic for a second serial port for the Minisport. The electrical part is pretty simple (the 14C88 and 14C89 do all the work), the tricky part was the mechanical assembly. I built it on a small piece of perfboard, and carefully matched the 16 pin header so it slides right into the modem slot. Since the 8 pin jack was

a lot bigger than the phone jack that is supposed to plug into the modem,
I cut away part of the modem slot cover to provide access.





Note: I terminated the RS-232 in an 8-pin modular connector, using
a pinout to match an existing cable. Since the cable didn't have both
DCD and DSR, I tied them together at the minisport side. There is another
receiver available if you want to bring DCD out to pin 8 of the DB-25
connector."

73, Brian Mork (Opus-OVH)   KA9SNF@wb7nnf.#spokn.wa.usa
                              Internet BMORK@opus-ovh.spk.wa.us
                              6006-B Eaker, Fairchild, WA 99011

Brian Mork   Internet bmork@opus-ovh.spk.wa.us
 . . . .   Amateur Radio ka9snf@wb7nnf.#spokn.wa.usa
.. . ..   USMail 6006-B Eaker, Fairchild, WA 99011

End of Packet-Radio Digest V93 #201
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